Listing of Claims:

1. (Currently amended) A damascene method capable of avoiding copper extrusion, the damascene method comprising:

providing a semiconductor wafer including a substrate with at least one metal layer on the substrate;

depositing a dielectric layer on the metal layer;

forming a damascene recess structure having an opening exposing a portion of the metal layer in the dielectric layer;

performing ~~a degas~~ an annealing step to ~~make gas escape~~ remove trapped gas from the dielectric layer;

forming a barrier layer on portions of the exposed surface of the metal layer and on the damascene recess structure; and

forming a conductive layer on the barrier layer.

2. (Currently amended) The method of claim 1 wherein the trapped gas ~~escaping from the dielectric layer~~ comprises fluorine-containing gas.

3. (Currently amended) The method of claim 1 wherein the ~~degas~~ annealing step is ~~an anneal step by heating to~~ performed at a temperature in a range between 200℃ to 300℃.

4. (Original) The method of claim 1 wherein a passivation layer is formed between the metal layer and the dielectric layer.

5. (Original) The method of claim 4 wherein the passivation layer is substantially made from silicon nitride.

6. (Original) The method of claim 1 wherein the dielectric layer is a laminate compound

layer comprising a first low-k dielectric, a stop layer over the first low-k dielectric, a second low-k dielectric, and a hard mask layer.

7. (Original). The method of claim 1 wherein the metal layer is made of copper or tungsten.

8. (Original) The method of claim 1 wherein the damascene recess structure is a dual damascene recess.

9. (Currently amended) A damascene method capable of avoiding conductive material extrusion, the damascene method comprising:

providing a substrate;

forming a plurality of devices on the substrate;

forming an interlayer dielectric to encapsulate the plurality of devices;

forming a plurality of conductive plugs in the interlayer dielectric to connect the devices on the substrate;

forming a dielectric layer having an embedded metal layer therein over the interlayer dielectric;

forming a low-k dielectric film over the dielectric layer;

etching a damascene recess structure in the low-k dielectric film, the damascene recess structure communicating the embedded metal layer;

executing ~~a degas~~ an annealing step to expel gas contained by the low-k dielectric film;

forming a barrier layer covering surface of the damascene recess structure and surface of the low-k dielectric film; and

depositing a conductive layer over the barrier layer.

10. (Currently amended) The method of claim 9 wherein the gas contained by the low-k

dielectric film is fluorine-containing gas.

11. (Currently amended) The method of claim 9 wherein the ~~degas step is an~~ annealing step is executed within a temperature range between 200℃ to 300℃.

12. (Original) The method of claim 9 wherein the conductive layer is a copper layer.

13. (Original) The method of claim 9 wherein between the embedded metal layer and the low-k dielectric layer, a passivation layer is formed.

14. (Original) The method of claim 13 wherein the passivation layer is substantially made from silicon nitride.

15. (Original) The method of claim 9 wherein the low-k dielectric layer has a dielectric constant (k) that is less than 2.9.

16. (Original) The method of claim 9 wherein the low-k dielectric film is a laminate compound layer comprising a first low-k dielectric, a stop layer over the first low-k dielectric, a second low-k dielectric, and a hard mask layer.

17. (Original) The method of claim 9 wherein the damascene recess structure is a dual damascene recess.